

## MEMORY CELL AND METHOD FOR FABRICATING SAME

### Field of the Invention

5       The present disclosure relates to a semiconductor device and a method for fabricating same, and more specifically, to a memory cell including an insulating layer for storing electrons having a multi-layer structure and a method of fabricating same.

### Background of the Invention

10       A silicon-oxide-nitride-oxide-silicon (SONOS) memory device has a similar structure to a metal-oxide-semiconductor (MOS) transistor and utilizes an insulating layer having a multi-layer structure as a gate insulating layer. The insulating layer may, for example, include a tunnel  
15   insulating layer, a charge trapping layer and a blocking insulating layer. The charge trapping layer is conventionally formed of silicon nitride. The SONOS memory device may write or erase information using Fowler-Nordheim tunneling (F-N tunneling) or hot carrier injection. U.S. Patent No. 5,768,192 to Eitan entitled "NON-VOLATILE SEMICONDUCTOR  
20   MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING" relates to writing or erasing information by hot carrier injection.

      Fig. 1 is a cross-sectional view showing a conventional SONOS memory cell.

      Referring to Fig. 1, a conventional SONOS memory cell includes  
25   source and drain regions 12 and 14 formed in a semiconductor substrate 10

and a gate electrode 22 formed on a channel region defined in the semiconductor substrate 10 between the source and drain regions 12 and 14. An insulating layer having a multi-layer structure is disposed between the gate electrode 22 and the semiconductor substrate 10 and includes a tunnel  
5 oxide layer 16, a charge trapping layer 18 and a blocking insulating layer 20.

When ground, gate and drain voltages are applied to the source region 12, the gate electrode 22 and the drain region 14, respectively, accelerated or hot charge carriers develop in the channel region near the  
10 drain region 14 and electrons or holes are trapped in a charge storage region 24. The polarity of the gate and drain voltage, can define a charge storage region 24 where electrons are trapped.

In the conventional SONOS memory cell, a charge storage region is not defined, but determined depending on the region where hot carrier  
15 injection occurs. Therefore, if the region where electrons are injected is different from the region where holes are injected, threshold voltage can vary due to repeating writing or erasing cycles. In addition, the charge trapping layer 18 where the electrons are trapped is positioned between the charge storage regions 24, such that electrons with thermal energy move  
20 parallel along the charge trapping layer 18. Therefore, data identification between the two charge storage regions 24 is deteriorated. Further, because an area of the charge trapping layer 18 is determined by a photolithographic process, distribution of a trap site can increase.

### Summary of the Invention

A memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance, a channel region defined between the source region and the drain region, a first charge storage layer formed on the channel region adjacent the source region, a second charge storage layer formed on the channel region adjacent the drain region, a gate insulating layer formed on the channel region between the first and second charge storage layers, and a gate electrode formed on the gate insulating layer and the first and second charge storage layers.

Each of the first and second charge storage layers may include a tunnel oxide layer, a charge trapping layer and a blocking insulating layer in a stacked formation. The gate insulating layer may have an equivalent oxide thickness less than a thickness of each one of the first and second charge storage layers. The gate insulating layer may comprise sidewalls that are aligned with sidewalls of the first and second charge storage layers.

The gate electrode may comprise a gate pattern formed on the gate insulating layer, and a gate sidewall pattern formed on each of the first and second charge storage layers.

Another memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance, a channel region defined between the source region and the drain region, at least two charge storage layers

formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region, a gate insulting layer formed on the channel region between the at least two charge storage layers, a gate pattern formed on the gate insulting layer, at least one lower sidewall pattern formed on at least one of the at least two charge storage layers, and at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one upper sidewall pattern electrically contacts the at least one lower sidewall pattern and the gate pattern.

Another memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance, a channel region defined between the source region and the drain region, at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region, a gate insulting layer formed on the channel region between the at least two charge storage layers, a gate pattern formed on the gate insulting layer, at least one lower sidewall pattern formed on at least one of the at least two charge storage layers, and at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one lower sidewall pattern is electrically insulated from the at least one upper sidewall pattern and the gate pattern.

The memory cell may also include at least one inter-gate insulating layer interposed between the at least one lower sidewall pattern and the at

least one upper sidewall pattern. A voltage may be independently applied to the gate pattern and to the at least one lower sidewall pattern,

A method for fabricating a memory cell, in accordance with an embodiment of the present invention, comprises stacking an insulating layer, a lower conductive layer and a mask layer on a semiconductor substrate, patterning the mask layer, the lower conductive layer and the insulating layer to form a gap region, forming a gate oxide layer on exposed surfaces of the semiconductor substrate and the lower conductive layer in the gap region, forming a gate pattern on the gate oxide layer for filling the gap region, removing the mask layer to expose sidewall portions of the gate pattern, forming an upper sidewall pattern on each exposed sidewall portion of the gate pattern, patterning the lower conductive layer and the insulating layer to form a lower sidewall pattern and a charge storage layer under each upper sidewall pattern, wherein the gate pattern and each upper sidewall pattern is used as an etching mask.

Another method for fabricating a memory cell, in accordance with an embodiment of the present invention, comprises stacking an insulating layer, a lower conductive layer, an interlayer insulating layer and a mask layer on a semiconductor substrate, patterning the mask layer, the interlayer insulating layer, the lower conductive layer and the insulating layer to form a gap region, forming a gate oxide layer on exposed surfaces of the semiconductor substrate and the lower conductive layer in the gap region, forming a gate pattern on the gate oxide layer for filling the gap region, removing the mask layer to expose the interlayer insulating layer and sidewall portions of the gate pattern, forming an upper sidewall pattern on

each exposed sidewall portion of the gate pattern and on the interlayer insulting layer, patterning the interlayer insulting layer, the lower conductive layer and the insulting layer to form an inter-gate insulting layer, a lower sidewall pattern and a charge storage layer under each upper sidewall pattern, wherein the gate pattern and each upper sidewall pattern is used as an etching mask, and forming a source region and a drain region in the semiconductor substrate adjacent a first charge storage layer and a second charge storage layer, respectively, wherein the gate pattern and each upper sidewall pattern is used as an ion implantation mask.

Impurities may be doped into an exposed portion of the semiconductor substrate in the gap region to form a channel region. Forming the upper sidewall pattern on each exposed sidewall portion may comprise forming an upper conductive layer on the semiconductor substrate after removing the mask layer, and anisotropically etching the upper conductive layer to expose the lower conductive layer or the interlayer insulting layer.

#### Brief Description of the Drawings

Preferred embodiments of the invention may be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings in which:

Fig. 1 is a cross-sectional view showing conventional SONOS memory cell;

Fig. 2 is a cross-sectional view showing a memory cell in accordance with an embodiment of the present invention;

Figs. 3 through 7 are cross-sectional views for illustrating a method for fabricating a memory cell in accordance with an embodiment of the present invention;

Fig. 8 is a cross-sectional view showing a memory cell in  
5 accordance with an embodiment of the present invention; and

Figs. 9 through 14 are cross-sectional views for illustrating a method for fabricating a memory cell in accordance with an embodiment of the present invention.

#### 10 Detailed Description of the Preferred Embodiments

Preferred embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. This invention may, however, be embodied in different forms and should not be constructed as limited to the embodiments set forth herein. Rather, these  
15 embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the  
20 other layer or substrate or intervening layers may also be present. Like numbers refer to like elements throughout the specification.

Fig. 2 is a cross-sectional view showing a memory cell in accordance with an embodiment of the present invention.

Referring to Fig. 2, a SONOS memory cell in accordance with an  
25 embodiment of the present invention includes a source region 74s and a

drain region 74d formed in a semiconductor substrate 50. Channel region 76 is located between the source region 74s and the drain region 74d. A gate insulating layer 64 and a charge storage insulating layer 72 are formed on the channel region 76, and a gate electrode 70 is formed on the gate insulating layer 64 and the charge storage insulating layer 72.

As shown in Fig. 2, the charge storage insulating layer 72 is formed on the channel region 76 adjacent the source and drain regions 74s and 74d. The gate insulating layer 64 includes sidewalls 64s which are aligned with sidewalls of the charge storage insulating layer 72 and extend in the vertical direction. The gate electrode 70 includes a gate pattern 66 formed on the gate insulating layer 64 and lower and upper sidewall patterns 58a and 68a, respectively. The lower and upper sidewall patterns 58a and 68a are stacked next to the sidewalls of the gate pattern 66 and on the charge storage insulating layer 72. A silicide layer 66s may be formed on top of the gate pattern 66. The gate insulating layer 64 extends to the region between the lower sidewall pattern 58a and the gate pattern 66. The gate pattern 66, the upper sidewall pattern 68a and the lower sidewall pattern 58a include a conductive layer and are electrically connected with one another.

In the memory cell shown in Fig. 2, data is written or erased by applying gate, source and drain voltages  $V_g$ ,  $V_s$ , and  $V_d$  to the gate electrode 70, the source region 74s and drain region 74d, respectively. One of the charge storage insulating layers 72 is selected according to the voltage difference between the source and the drain voltages  $V_s$  and  $V_d$ .

Figs. 3 through 7 are cross-sectional views for illustrating a method for fabricating a memory cell in accordance with an embodiment of the



present invention.

Referring to Fig. 3, a tunnel oxide layer 52, a charge trapping layer 54 and a blocking insulating layer 56 are stacked on a semiconductor substrate 50 to form an insulating layer having a multi-layer structure. A lower conductive layer 58 and a hard mask layer 60 are formed on the multi-layered insulating layer. The multi-layered insulating layer may be formed of, for example, silicon oxide, silicon nitride and silicon oxide that are stacked. The lower conductive layer 58 may be formed of polysilicon. The tunnel oxide layer 52 is one of metal oxide, silicon oxynitride, silicon oxide and a stacked multi-layer structure of the metal oxide, silicon oxynitride and silicon oxide.

Referring to Fig. 4, the hard mask layer 60, the lower conductive layer 58 and the insulating layer having the multi-layer structure are successively patterned to form a gap region 62. A gate insulating layer 64 is formed on surfaces of the semiconductor substrate 50 and the lower conductive layer 58, which are exposed in the gap region 62. The gate insulating layer 64 may be formed of thermal oxide or chemical vapor deposition (CVD) oxide having a thickness from approximately 80Å to approximately 150Å. Before and after forming the gate insulating layer 64, impurities may be doped into the semiconductor substrate 50 for adjusting threshold voltage using the hard mask layer 60 as an ion implantation mask.

Referring to Fig. 5, a gate conductive layer filling the gap region 62 is formed on the hard mask layer 60 and then polished by a chemical mechanical polishing process to form a gate pattern 66 filling the gap region 62. A silicidation process may be applied to the semiconductor

substrate 50 with the gate pattern 66, thereby forming a silicide layer 66s on the gate pattern 66.

Referring to Fig. 6, a hard mask layer 60 is removed. The hard mask layer 60 may be formed of a silicon nitride layer and removed by wet etching using ammonia or phosphoric acid. An upper conductive layer 68 is formed on an entire surface of a resulting structure of the substrate 50. The thickness of the upper conductive layer 68 may be adjusted according to the cell characteristics. The thickness of the upper conductive layer 68 is a factor in determining the width of the charge storage region of the memory cell.

Referring to Fig. 7, the upper conductive layer 68 and the lower conductive layer 58 are anisotropically etched to form a lower sidewall pattern 58a and an upper sidewall pattern 68a, which are stacked adjacent to sidewalls of the gate pattern 66. Using the gate pattern 66 and the upper sidewall pattern 68a as an etch mask, the multi-layered insulating layer is patterned to form the charge storage insulating layer 72 including tunnel oxide layer 52, charge trapping layer 54 and blocking insulating layer 56, which are stacked. Impurities are doped into the semiconductor substrate 50 to form source region 74s and drain region 74d adjacent the charge storage insulating layer 72.

Fig. 8 is a cross-sectional view showing a memory cell in accordance with an embodiment of the present invention.

Referring to Fig. 8, a SONOS memory cell includes source and drain regions 74s and 74d formed in a semiconductor substrate 50. Channel region 76 is located between the source and drain regions 74s and 74d. A

gate insulating layer 64 and a charge storage insulating layer 72 are formed on the channel region 76, and a gate electrode 70 is formed on the gate insulating layer 64 and the charge storage insulating layer 72. The charge storage insulating layer 72 is formed on the channel region 76 adjacent the source and drain regions 74s and 74d. The gate insulating layer 64 includes sidewalls 64s which are aligned with sidewalls of charge storage insulating layer 72 and extend in the vertical direction. The gate electrode 70 includes a gate pattern 66 formed on the gate insulating layer 64 and lower and upper sidewall patterns 58a and 68a, respectively, that are stacked next to the sidewalls of the gate pattern 66. The gate electrode 70 also includes an inter-gate insulating layer 59a interposed between the lower and upper sidewall patterns 58a and 68a. A silicide layer 66s may be formed on top of the gate pattern 66. The gate insulating layer 64 extends to the region between the lower sidewall pattern 58a and the gate pattern 66 and connects to the inter-gate insulating layer 59a. As a result, the lower sidewall pattern 58a is insulated from the gate pattern 66 and the upper sidewall pattern 68a.

In the memory cell shown in Fig. 8, data is written or erased by applying first gate, second gate, source and drain voltages  $V_g$ ,  $V_f$ ,  $V_s$ , and  $V_d$  to the gate pattern 66, the lower sidewall pattern 58a, the source region 74s and drain region 74d, respectively. One of the charge storage insulating layers 72 is selected according to the voltage difference between the source and the drain voltages  $V_s$  and  $V_d$ . Low voltage for forming an inversion layer in the channel region 76 may be applied to the gate pattern 66 and to the lower sidewall pattern 58a on the non-selected charge storage insulating layer 72, while high voltage for generating hot carriers may be applied to

the lower sidewall pattern 58a on the selected charge storage insulating layer 72. Therefore, data retention by the non-selected charge storage insulating layer 72 is improved during writing and erasing operations.

Figs. 9 through 14 are cross-sectional views for illustrating a method for fabricating a memory cell in accordance with an embodiment of the present invention.

Referring to Fig. 9, a tunnel oxide layer 52, a charge trapping layer 54 and a blocking insulating layer 56 are stacked on a semiconductor substrate 50 to form a multi-layered insulating layer. A lower conductive layer 58, an interlayer insulating layer 59 and a hard mask layer 60 are formed on the insulating layer having the multi-layer structure. The multi-layered insulating layer may be formed of, for example, stacked layers including silicon oxide, silicon nitride and silicon oxide. The lower conductive layer 58 may be formed of polysilicon. The tunnel oxide layer 52 may be formed of one of metal oxide, silicon oxynitride, silicon oxide and a stacked multi-layer structure including metal oxide, silicon oxynitride and silicon oxide.

Referring to Fig. 10, the hard mask layer 60, the lower conductive layer 58, the interlayer insulating layer 59 and the insulating layer including the plurality of layers are successively patterned to form a gap region 62. A gate insulating layer 64 is formed on surfaces of the semiconductor substrate 50 and the lower conductive layer 58, which are exposed in the gap region 62. The gate insulating layer 64 may be formed of thermal oxide or CVD oxide having a thickness from approximately 80Å to approximately 150Å. The gate insulating layer 64 extends along the

sidewall of the gap region 62 and connects to the interlayer insulating layer 59. Before and after forming the gate insulating layer 64, using the hard mask layer 60 as an ion implantation mask, impurities may be doped into the semiconductor substrate 50 for adjusting threshold voltage.

5 Referring to Fig. 11, a gate conductive layer filling the gap region 62 is formed on the hard mask layer 60 and then polished by a chemical mechanical polishing process to form a gate pattern 66 filling the gap region 62. A silicidation process may be applied to the semiconductor substrate 50 including the gate pattern 66, thereby forming a silicide layer  
10 66s on the gate pattern 66.

Referring to Fig. 12, a hard mask layer 60 is removed. The hard mask layer 60 may be formed of a silicon nitride layer and removed by wet etching using an ammonia or phosphoric acid solution. An upper conductive layer 68 is formed on an entire surface of a resulting structure of the  
15 substrate 50 without the hard mask layer 60. The thickness of the upper conductive layer 68 may be properly adjusted according to cell characteristics. The thickness of the upper conductive layer 68 is a factor in determining width of the charge storage region of the memory cell.

Referring to Fig. 13, the upper conductive layer 68 is anisotropically  
20 etched to form an upper sidewall pattern 68a on sidewalls of the gate pattern 66. Using the gate pattern 66 and the upper sidewall pattern 68a as an etch mask, the interlayer insulating layer 59 is patterned to form an inter-gate insulating layer 59a.

Referring to Fig. 14, the lower conductive layer 58 is anisotropically  
25 etched to form lower sidewall patterns 58a under the inter-gate insulating

layer 59a. Using the gate pattern 66 and the upper sidewall pattern 68a as an etch mask, the insulating layer having a multi-layer structure is patterned to form a charge storage insulating layer 72 including a tunnel oxide layer 52, charge trapping layer 54 and blocking insulating layer 56, which are stacked. Impurities are doped into the semiconductor substrate 50 to form source region 74s and drain region 74d adjacent the charge storage insulating layer 72.

A conventional SONOS memory cell may include a charge storage insulating layer formed on a channel region, wherein the charge storage insulating layer has an equivalent oxide thickness (EOT) that is larger than a thickness of gate insulating layer. In contrast, according to an embodiment of the present invention, a charge storage insulating layer is formed only on the regions adjacent the source and drain regions, and a thin gate insulating layer is formed on the remaining portion of the channel region. With this configuration, the thin gate insulating layer has an EOT that is less than a thickness of the charge storage insulating layer.

In accordance with an embodiment of the present invention, the charge storage insulating layer is formed only on the region where electrons are trapped, thereby improving an operating rate of the memory cell. In addition, a width of the charge storage insulating layer can be controlled to have a uniform thickness, such that distribution of the cell can be reduced. The charge storage insulating layer may be formed in separate parts on different portions on the channel region (e.g., adjacent the drain and storage regions), thereby improving data identification between the charge storage regions. Furthermore, the width of the charge storage insulating layer along

the channel length can be minute, such that electrons and holes can be injected into the same region.

Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those precise embodiments, and that  
5 various other changes and modifications may be affected therein by one of ordinary skill in the related art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended  
10 claims.